Interference Search History Printout MT

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	0	(semiconductor near package and die and substrate and coplanar and active near surface and inactive near surface).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:04
L2	1	(semiconductor near package and die and substrate and coplanar and active near surface).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:05
L3	0	(semiconductor near package and die and substrate and coplanar and inactive near surface and interconnect).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:06
L4	0	(semiconductor near package and die and substrate and coplanar and inactive adj surface and interconnect).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:06
L5	0	(semiconductor near package and die and substrate and coplanar and inactive adj surface).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:06
L6	22	(semiconductor near package and die and substrate and coplanar). CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:08
L7	0	(semiconductor near package and die and substrate and coplanar and four near perpheral).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:08
L8	0	(semiconductor and die and substrate and coplanar and four near perpheral).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:09
L9	0	(semiconductor and die and substrate and coplanar and four near peripheral).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:09
L10	15	(semiconductor near package and semiconductor near die and substrate and coplanar).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:11
L11	2	(semiconductor near package and die and substrate and coplanar and peripheral).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:12
L12	0	(semiconductor and bond near fingers and ball near lands and die and substrate and peripheral).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:14

L13	0	(semiconductor and bond near fingers and die and substrate and peripheral).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:14
L14	96	(semiconductor and die and substrate and coplanar).CLM.	US-PGPUB; USPAT; USOCR; EPO; JPO	OR	OFF	2005/09/02 12:14